***Logistic Regression V1***

**Accuracy vs. Latency vs. EXP Iterations:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **EXP Iterations** | Accuracy  (%) | Time Period | ARM Cortex  Latency (ns) | FPGA Latency (ns) |
| 1 | 54.96 | 3.2n |  |  |
| 2 | 45.0 | 3.2n |  |  |
| 3 | 76.15 | 3.2n |  |  |
| 4 | 52.98 | 3.2n |  |  |
| 5 | 76.15 | 3.2n |  |  |
| 6 | 53.64 | 3.2n |  |  |
| 7 | 76.15 | 3.2n |  |  |
| 8 | 59.60 | 3.2n |  |  |

***Logistic Regression V2***

**Accuracy vs. Latency vs. Order:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Order** | Accuracy  (%) | FPGA Latency (ns) | ARM Cortex  Latency (s) |
| 1 | 50.42 | 3.16n | **0.018** |
| 2 | 50.42 | 3.17n | **0.021** |
| 3 | 82.71 | 3.2n | **0.024** |
| 4 | 82.71 | 3.3n | **0.026** |

|  |
| --- |
| **Algorithm1** Modified Logistic Regression Algorithm |
| **Input:** Cp-close prices; Hp-High prices; Lp -High prices; N-Total number of Test Data; TrainC-Trained Coefficients; FX-Input Feature; respectively X =1,2  **Output:** D signal  **for** i = 0 to N **do**  F1(i)  = Hp (i) - Cp (i);  F2(i)  = Cp (i) - Lp (i);  Intercept = TrainC1<<24;  Coeff1(i) = (TrainC2\* F1(i)) <<24;  Coeff2(i) = (TrainC3\* F2(i)) <<24;  x(i) = Intercept + Coeff1(i) – Coeff2(i);  x(i) = x(i)>>22;  Exp(i) = 1+x(i) – ((x(i)^2)/2) + ((x(i)^3)/6) +………+((x(i)^n)/(N-1)!);  **if** Exp(i) < 1 **then**  D(i) = 1;  **else**  D(i) = 0;  **end if**  **end for** |
|  |